ROBOTS IN ASSISTED
LIVING ENVIRONMENTS

UNOBTRUSIVE, EFFICIENT, RELIABLE AND MODULAR SOLUTIONS FOR INDEPENDENT AGEING

Research Innovation Action

Project Number: 643892 Start Date of Project: 01/04/2015 Duration: 36 months

DELIVERABLE 4.4

Robust and Energy Efficient Hardware Components I

Dissemination Level	**Public**
Due Date of Deliverable	Project Month 15, 1 July 2016
Actual Submission Date	5 April 2917
Work Package	WP4*: Components for elder monitoring and caring*
Task	T4.2: *Embedded device design and development*
Lead Beneficiary	AVN
Contributing beneficiaries	TWG, RUB
Type	DEM
Status	Submitted
Version	Final

Project funded by the European Union's Horizon 2020 Research and Innovation Actions

Abstract

The first version of this deliverable presents a library of dedicated SW-HW components required to integrate the Zynq FPGA board to the on-robot processing unit, to setup the FPGA with a fully-functional embedded Linux distribution, to bring up the ROS operating system on top of the embedded Linux, and to build the framework for developing FPGA HW accelerators (and connect them efficiently with the ROS system).

History and Contributors

Ver	Date	Description	Contributors
00	25 May 2016	Document structure	AVN
01	22 Jun 2016	Section 1	AVN
02	6 Jul 2016	Added pointers to source code for FPGA implementations and other minor	AVN, TWG, RUB
04	17 Mar 2017	Evaluation completed	TWG, AVN
05	5 Apr 2017	Internal peer review	NCSR-D
06	5 Apr 2017	Addresses peer review comments	AVN
Fin	5 Apr 2017	Final preparations and submission.	NCSR-D

Abbreviations and Acronyms

SoC	System on Chip
ROS	Robotic Operating System
ADL	Activities of Daily Life
HDMI	High-Definition Multimedia Interface
DHCP	Dynamic Host Configuration Protocol

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1 INTRODUCTION

1.1 Purpose and scope

This deliverable is a demonstration of the RADIO approach for increasing the power efficiency and robustness of the system by using dedicated hardware components to implement in a SoC-based FPGA some of the data processing methods developed in WP3. The scope of delivery includes

The scope of delivery is the source code given in Table 1 (Section 2) and that this code has been physically prototyped on a PicoZed FPGA (Figure 2, Section 2) and evaluated. The evaluation results are reported in D4.2.

1.2 Approach

This deliverable is prepared within Task 4.2 that designs and prototypes embedded hardware components that implement selected data processing methods among those developed in WP3. The end-result is a library of dedicated SW and HW components. To develop the hardware components, RUB improved the hardware architecture for accelerating image processing algorithms. With the improved architecture, several image processing algorithms can be implemented without additional engineering effort and dynamically loaded on the FPGA. AVN and RUB used this new architecture to accelerate the motion detection prototype (developed in WP3). TWG designed, prototyped, and evaluated FPGA components. Several performance measurements were made in order to maximize the speedup of the provided algorithm. Several optimization steps have been taken through the high level synthesis software of Xilinx Vivado HLS.

Special emphasis was given to prepare a library of dedicated SW-HW components required to integrate the Zynq FPGA board to the on-robot processing unit, to setup the FPGA with a fully-functional embedded Linux distribution, to bring up the ROS operating system on top of the embedded Linux, and to build the framework for developing FPGA HW accelerators (and connect them efficiently with the ROS system).

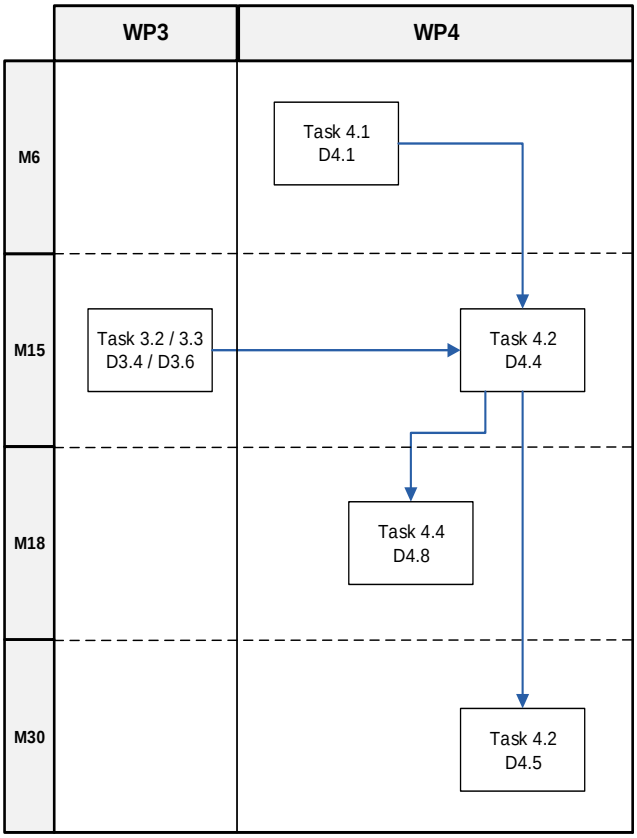

Figure 1: Relation to other Work Packages and Deliverables

1.3 Relation to other Work Packages and Deliverables

This deliverable is prepared following the *Architecture for extending smart homes with robotic platforms I* (D4.1). D4.4 implements in hardware methods developed in D3.4 *ADL recognition methods* and is also aware of the system networking developed in D3.6 *Communication, processing and security efficiency methods*.

The robust and energy efficient hardware components described in this deliverable are used by *Task 4.4: Smart home design and integration* in order to prepare the *Integrated smart home with robotic platform* (D4.8).

The next iteration of this deliverable is D4.5, due M30.

2 PROTOTYPE

Figure 2 presents the FPGA-based architecture of the system. It uses the Zynq processing system consisting of a ARM Cortex-A9 Dual-Core CPU and the implementation for video direct memory access (VDMA).

The Zynq processing system receives the image over the network via ROS messages. The image must then be sent to the image processing hardware via memory mapping. Them memory mapped file is hereby directly accessed by the VDMA. Additionally, the VDMA needs to be configured to also provide a memory mapped output image, if necessary. The image processing hardware expects the AXI Stream protocol as input. However, the high-performance port of the Zynq only communicates via AXI3. The AXI3 protocol is converted to AXI4 through the AXI interconnect device which is then converted to AXI Stream by the VDMA.

Table 1 gives the HW-SW sources developed as part of this deliverable

Table 1: Code Repositories

Repository	Description
https://github.com/radio-project-eu/hwaccel_radio	Source code (and project configuration) that allows to build the hardware in PicoZed needed to interface with the robot, bring up ROS and implement algorithm accelerators. In order to build it you will need the Xilinx Vivado tool suite (and the PicoZed so that you can program and test the image)
https://github.com/radio-project-eu/Zedboard_Linaro_Radio	A fully functional Linaro embedded Linux distribution with support for HDMI screens, with keyboard and mouse for the FPGA Zedboards. Network connection is configured to DHCP protocol. Server-side ssh and sftp is also installed (username and password: linaro).

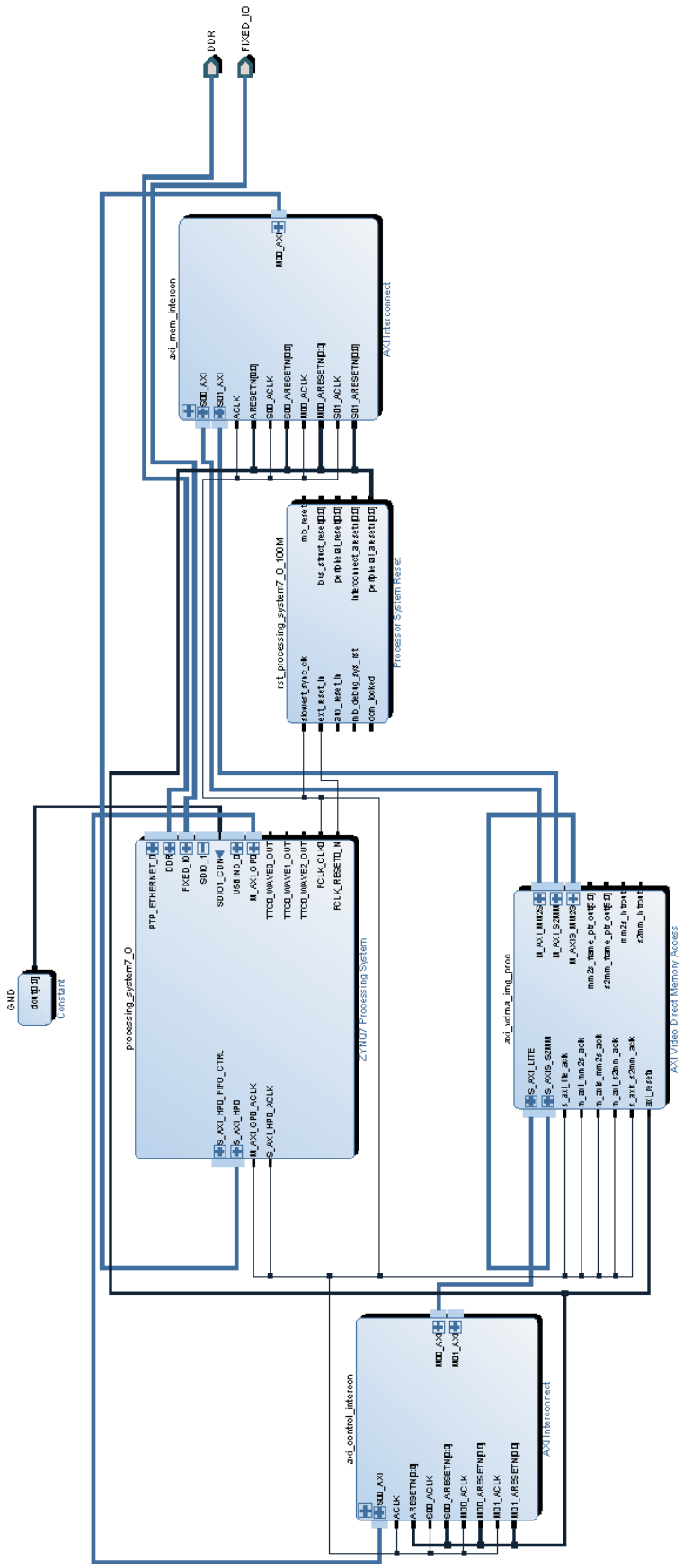

Figure 2: Example Architecture of a FPGA HW Accelatator

3 NEXT STEPS

The initial architecture of the RADIO robot is ready to accept the developed components. There is an FPGA unit, connected to the robot CPU and –through this- to all subsystems of the robot. The fact that all connections are through the CPU means that the CPU cannot be completely turned off, as it is need for:

- Getting the images from the camera to the FPGA memory
- Receiving notification from the beacons
- Interfacing to the WiFi and Smart-home networks

To minimize the impact of this, perhaps the most useful additions would be:

(a) to develop a direct connection between the camera and the FPGA so that images do not have to be copied by the CPU. This will allow much more extensive pre-processing in the FPGA while the CPU is not consuming any energy at all

(b) to design a special smart-home node device which would bring notifications from smart-home sensors directly on the FPGA. This would allow all other subsystems to be at sleep mode, until some external event triggers activity

The prototyping of the dedicated HW components for the selected ADLs and the analysis of the results from their usage will be presented in the second version of this report in deliverable D4.5.